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ASIC for Hybrid Biosynthetic Infochemical Chemoreceiver

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Abstract— In this paper we report upon the design of an application-specific integrated circuit (ASIC) that forms part of a single-board implementation of a smart chemoreceiver within an infochemical communication system. The ASIC, comprising four differential surface acoustic wave resonator (SAWR) circuits, enables the sensing of odour blend ratios of either fruit volatiles or sex pheromones for insects. The ASIC chip has a digital interface to an FPGA containing a neuromorphic blend model developed in order to classify specific ratios of chemical compounds in the odour blends and used to control a mobile robot. The ASIC measures small changes in the resonant frequency of functionalized piezoelectric sensors with a resolution of 20 Hz and where the base SAW frequency is selected in the range of 60 to 969 MHz. The BiCMOS ASIC chip has dimensions 3 mm × 3 mm and was fabricated at AustiaMicroSystems (AMS). The smart chemoreceiver can be integrated with a chemoemitter to create a novel insect based infochemical communication system.

I. INTRODUCTION

This ASIC chip has been designed as part of an EU funded project [1] to demonstrate, in real-time, the neuromorphic processing of chemical sensor signals to extract blend specificity information in a system that emulates both insect olfaction and infochemical communication. The complete system consists of chemoemitter for the deployment of chemicals in specific ratios into the communication channel and chemoreceiver able not just to detect different chemicals but to recover their specific ratios. This system uses either biological sensors based on insect cells expressing relevant olfactory receptors or organic sensors based upon polymers.

Our current work presents an intermediate hybrid stage between previous system comprising PCBs and discrete components (Figures 1) and the final portable monolithic chemoreceiver device. It is capable of supporting experimental studies using an array of up to four biosensors to detect blends of chemical compounds and replaces the entire discrete sensor module shown in Figure 1(b).

The ASIC has been developed as a part of compact portable system with four chemical detection channels that can be placed on a mobile robot and interfaced to the back-end FPGA block where neuromorphic computation is carried out.

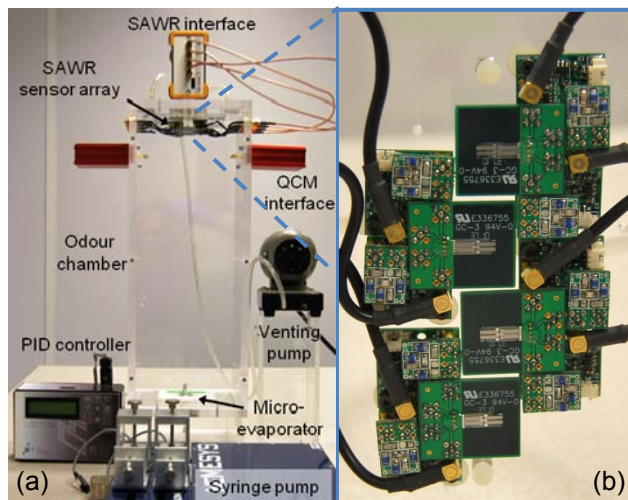


Figure 1: (a) Experimental setup for infochemical communication with micro-evaporator and SAWR chemo-receiver, and (b) the SAWR sensor array and its associated circuitry.

II. PROTOTYPE SYSTEM

Prior to the implementation of the ASIC system, an initial prototype system has been developed using discrete components, including SAWR sensors, filters, amplifier circuits and buffers as shown in the Figure 1b. The basic concept and preliminary results of biological sensors have been reported previously [2,3]. However, whilst performing measurements on discrete components it was realized that there were two main problems: (1) variation in the resonant frequencies of nominally identical SAW resonators and (2) drift of the resonant frequency over time with changes in ambient temperature and cell properties.

For a resonant system, small changes/differences in ideal closed-loop phase shift lead to a shift in the resonance frequency of the sensor and a change in the amplitude of the returned sensor signal [4]. As a result, it is evident that the acoustic resonator oscillator design should be tailored to compensate for the phase characteristics of the acoustic sensor. The drift in the normal oscillating frequency of an acoustic sensor is generally caused by parametric variation

due to temperature changes in either the SAW piezoelectric substrate or the circuit components.

III. VLSI CHEMORECEIVER INTEGRATION

In order to enhance the performance and accuracy of measurements in the SAW based biosensor system, the resonator circuitry which has been implemented using discrete components was replaced by a single VLSI chip. This ASIC chip can drive up to four pairs of differential SAWR sensors and can be interfaced to an FPGA containing a neuromorphic computational block. The entire ASIC oscillator chip is about 3 mm by 3 mm. Figure 2 shows a comparison of the discrete oscillator circuitry and the on-chip resonator circuitry, detailing the overall size of the two circuits. A Printed Circuit Board (PCB) has been designed as shown in the Figure 3, which forms a full hybrid system including the ASIC chip, and is currently being characterised using the SAW based sensor system. The PCB is a four layer board with grounding layers to reduce the cross-talk associated with high frequency signals. It also takes account of the phase shifts associated with the RF signal paths to the individual SAWR sensors.

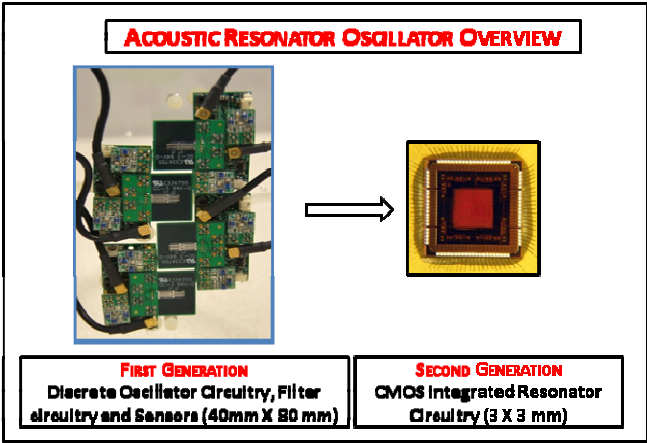


Figure 2: Acoustic resonator oscillator overview showing discrete circuitry and ASIC chip.

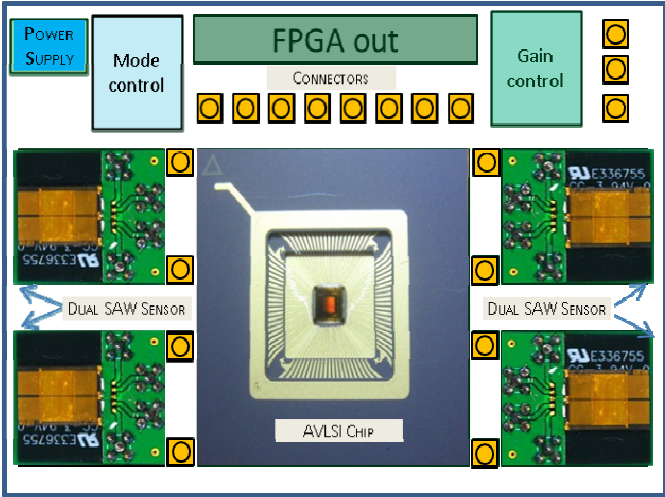


Figure 3: PCB schematic of the hybrid system including sensors, ASIC chip and digital output.

IV. ASIC IMPLEMENTATION

The ASIC has been developed using a 0.35μm 3.6V HF SiGe BiCMOS AMS process and has the capability of supporting up to eight single-ended channels (SAWRs). The chip can operate at frequencies of up to 1 GHz, has a number of on-chip mode selection options to compensate for any mismatching of the SAW oscillator frequencies and can readily measure frequencies to a 32-bit accuracy. Figure 4, shows the basic block diagram of the overall system.

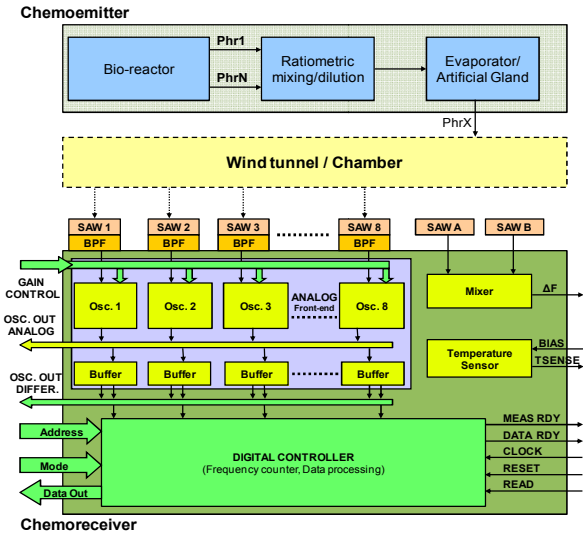


Figure 4: Schematic block diagram of the biosynthetic infochemical communication system.

It comprises of a chemoemitter in which a chemical blend is formulated and transmitted via an artificial evaporator/gland via a wind tunnel to the chemoreceiver. The chemoreceiver block contains SAW resonators that are placed outside the ASIC chip for detecting the transmitted blend. Sensor signals are processed by the chip and converted into digital form to be interfaced with a field-programmable gate array (FPGA) block, where the final neuromorphic computation is carried out and blend ratios recovered. A photograph of the fabricated 9 mm² chip is shown in Figure 5.

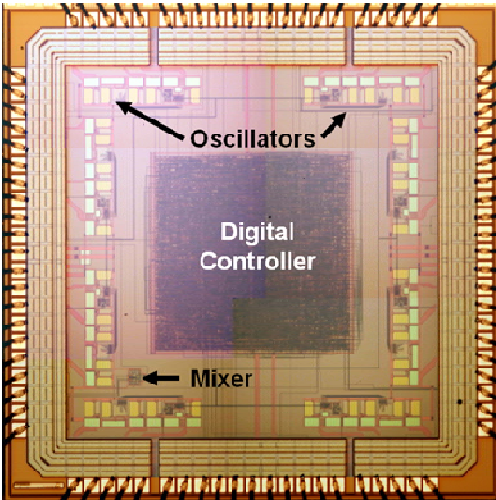


Figure 5: Composite micrograph of fabricated die.

A. The Oscillators

The basic building blocks for the oscillator circuit are shown in Figure 6. The oscillator was designed to ensure that it operated from 60 MHz to 869 MHz, and thus needed to have wideband capability. To achieve such performance capability and given that the oscillator needed to be configured for a 2-port SAW resonator together with selected AMS S35 BiCMOS process, a simple constant base current bias circuit topology with programmable gain control was found to be most suitable for this purpose. It is well known that such topology has two main limitations: (1) temperature stability and (2) bias resistance is R_b is dependent on the β parameter of the transistor. However, the latter issue can be resolved by programmable gain control and thus provides a degree of flexibility in terms of oscillation adjustment.

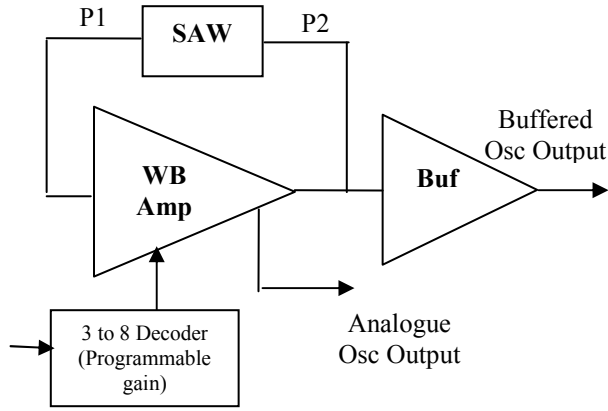


Figure 6: Oscillator Block

The actual amplifier (WB Amp, Figure 6) required 4-stages within the oscillator block and 2-stage buffering at the output that provides input to the digital control block where 32-bit frequency measurements are recorded. The final output buffer stage was designed to provide differential output and simulated to show its operation of more than 1GHz.

The ASIC provides seven levels of gain control options, ranging from 10 dB to 30dB, plus a choice of external control via resistor R (Figure 7).

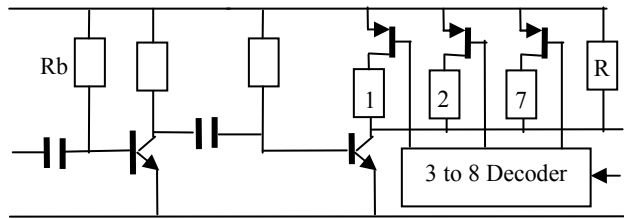


Figure 7: Wideband amplifier stage with programmable gain control

B. The Mixer

The ASIC chip also contains an analogue mixer based on Double Balanced Gilbert cell topology. This mixer has been included as a platform to check any mis-matching errors between two identical SAW devices or oscillators. Here, the differential output from the buffer stage can be applied to the mixer input to reduce noise interferences.

C. The Digital Controller

The digital controller block performs: (1) the frequency measurement on all eight channels to 32-bit accuracy, (2) computes difference between base and measured frequency (3) stores computed difference between two channels and (4) allows data to be read in 4×8 bit block.

The block diagram of the digital controller is shown below in Figure 8.

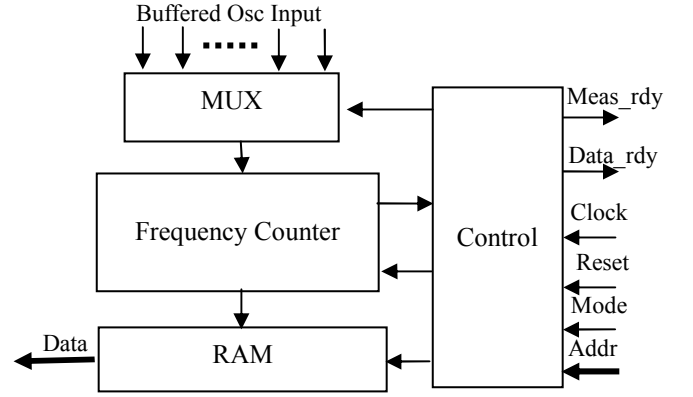


Figure 8: Digital controller

The controller is driven by a 10 MHz input clock. The frequency measurement is performed by gating clock at 50 ms. Here, the multiplexed oscillator input from each of the eight channels is applied to the counter to measure the frequency. With 50 ms gating we can achieve a measurement resolution of just 20 Hz. However, for increased resolution, it was found that a large divider is needed and this significantly increased the number of registers and logic gates required. The timing diagram of the frequency counter is shown in Figure 9.

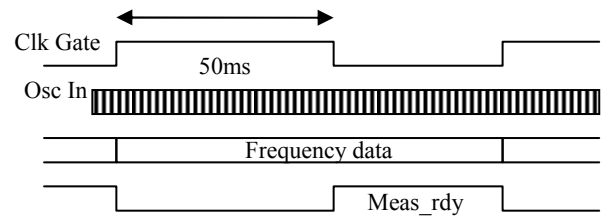


Figure 9: Gated frequency counter

V. SIMULATION RESULTS

Simulations of the oscillator blocks and the amplifier with programmable gain control are shown in Figure 10 for a base frequency of 869 MHz. The measured and actual outputs of the chip are given in Figure 11.

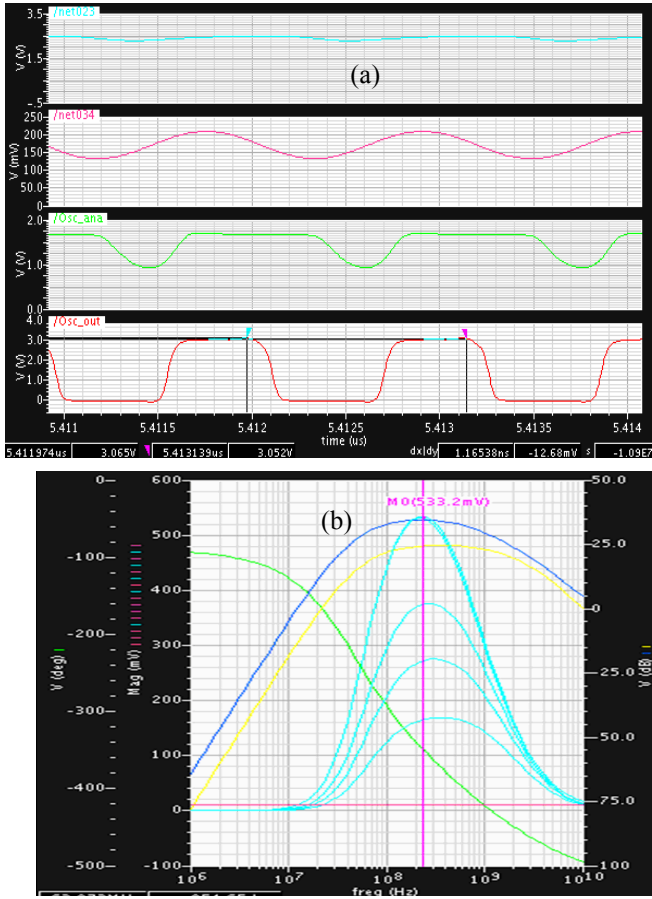


Figure 10: Simulation outputs: (a) the oscillator block at 869 MHz and (b) programmable gain control amplifier

The simulations shown in Figure 11, verified that it is possible to measure the input frequency accurately to 20 Hz resolution and retrieve the store the data in the addressable memory locations. The data can be read within the READ cycle. This process can be performed asynchronously when Meas_rdy is set, but it is recommended to synchronize with Data_rdy cyc

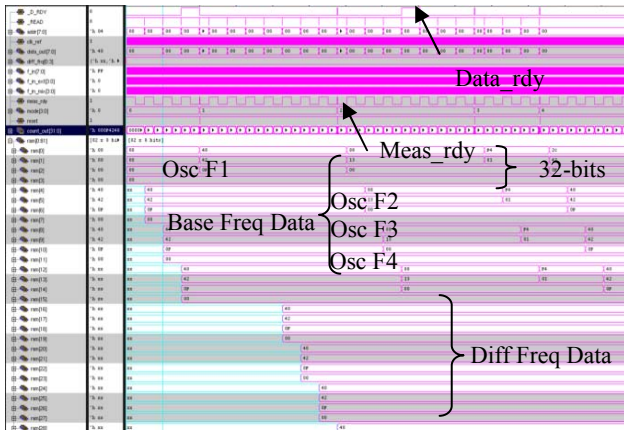


Figure 11: Measured actual and difference frequency data to 32-bit accuracy

The baseline oscillator miss-match is cancelled by initially storing the base frequency F1, F2 .. Fn in the register. During the measurement cycle, any drift in frequency can be monitored by checking the difference value during the calibration phase and then used to compensate for any error.

By selecting the appropriate mode on the ASIC chip, the difference between two oscillators can be calculated as $\Delta F = F1 - F2$ and stored in memory. For subsequent measurements, this data can be accessed and subtracted from any new measured frequency to remove the offset.

VI. CONCLUSIONS

An ASIC chip has been designed for application in an infochemical communication system employed 2-port SAW resonator sensors. The ASIC solution developed here shows that variation in the baseline oscillator frequencies and subsequent sensor drift can be digitally removed. This gives a greater flexibility in terms performing of more advanced on-chip signal processing. Furthermore, it allows the infochemical communication system to be miniaturized and serves as subsystem for further integration. The ultimate goal is to create a single chemoreceiver-on-a-chip solution for a mobile robot.

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